9T SRAM Cell with Improved Self-Controllable Voltage Level Circuits

B.S.K.Lakshmi
Mtech (VLSI Design)
Department of Electronics and Communication Engineering
Kakinada Institute of Engineering and technology,
korangi, India

R.Vinay Kumar
Mtech(VLSI Design)
Department of Electronics and Communication Engineering
Kakinada Institute of Engineering and technology,
korangi, India

***Abstract*— As the feature size of the transistor is scaled down, the threshold voltages of MOSFETs have been reduced thereby leakage power substantially increases. Furthermore, leakage is the only source of energy consumption in an idle circuit. A 0.25µm 9T SRAM which provides low leakage power is designed in this paper. A new leakage current reduction circuit called a "improved Self-controllable Voltage Level (SVL)" circuit is developed and included to reduce the leakage power of 9T SRAM. Simulation result of 9T SRAM with improved SVL design using TANNER tool shows the reduction in total average power. The Tanner T-spice simulation in standard 0.25µm CMOS technology confirms all results obtained for this paper.**

Keywords- Leakage Current; Low Power; SRAM; SVL; VLSI; USVL; LSVL.

I. INTRODUCTION

In modern high performance integrated circuits, more than 40% of the total active mode energy is consumed due to leakage currents [2], [3]. Furthermore, leakage is the only source of energy consumption in an idle circuit. SRAM arrays are important sources of leakage since the majority of transistors are utilized for on-chip memory in today's high performance microprocessors and systems-on-chips (SoCs) [6]. The design of a low leakage SRAM cell is, therefore, highly desirable.

In addition to the leakage power issues, the degradation of data stability in SRAM cells is another growing concern with the scaling of device dimensions and voltages in each new technology generation. The SRAM cell stability is further degraded due to process variations in deeply scaled CMOS technologies [1].

A new nine-transistor (9T) SRAM cell with reduced leakage power consumption and enhanced data stability is proposed in this paper. The leakage power consumption of the new SRAM cell is reduced by 99.99% as compared to the conventional nine-transistor (9T) SRAM cells. The 9T SRAM cell provides two separate data access mechanisms for the read and write operations. During a read operation, the data storage nodes are completely isolated from the bit lines.

II. 9T SRAM CELL DESIGN

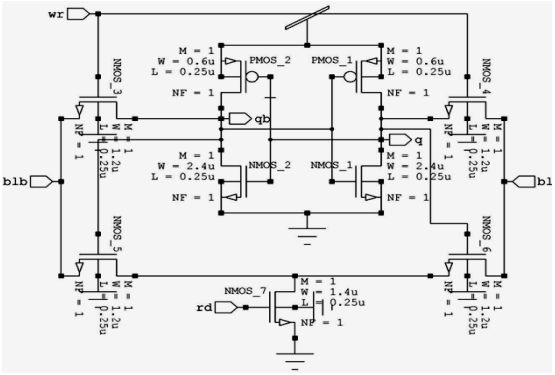

Figure 1. 9T SRAM CEL

The upper sub-circuit of the new memory cell is essentially a 9T SRAM cell with minimum sized devices (composed of N1, N2, N3, N4,N5,N6,N7, P1, and P2 with W=Wmin and L=Lmin). The two write access transistors (N3 and N4) are controlled by a write signal (WR).The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD) [1-3].

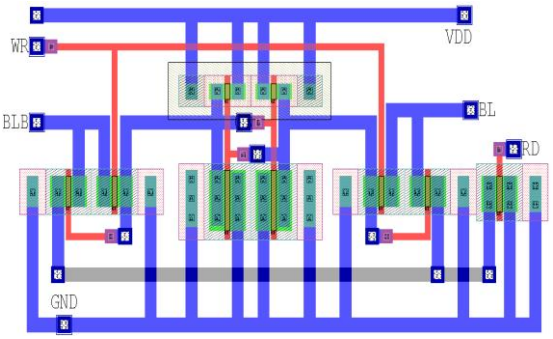

Figure 2. 9T SRAM Cell layout

A. 9T SRAM CELL Operation Table:

TABLE I. 9T SRAM CELL OPERATION

wr	rd	bl	blb	qbar	q	operation
0	0	x	x	0/1	1/0	hold
0	1	1	1	0/1	1/0	read
1	0	0	1	1	0	Write0
1	0	1	0	0	1	Write1

B. Write operation of 9T SRAM cell

During a write operation, WR signal transitions high while RD is maintained low, as shown in Fig. below N7 is cutoff. The two write access transistors N3 and N4 are turned on. In order to write a "0" to Node1, BL and BLB are discharged and charged, respectively.

A "0" is forced into the SRAM cell through N3. Alternatively, for writing a "0"to Node2, BL and BLB are charged and discharged, respectively. A"0"is forced onto Node2 through N4.

C. Read operation of 9T SRAM cell

During a read operation, RD signal transitions high while WR is maintained low, as illustrated in Fig. below. The read access transistor N7 is activated. Provided that Node1 stores "1", BL is discharged through N5 and N7. Alternatively, provided that Node2 stores"1", the complementary bit line (BLB) is discharged through N6 and N7.

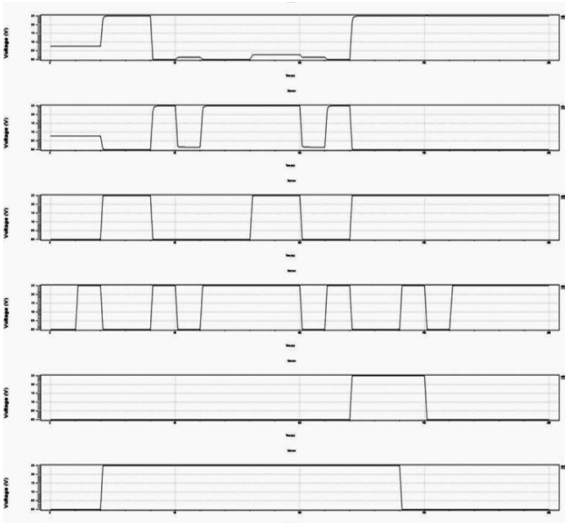

Figure 3. Simulation of 9T SRAM cell

III. SELF-CONTROLLABLE VOLTAGE LEVEL

There are two well-known techniques that reduce leakage power (Pst). One is to use a multi-threshold-voltage CMOS (MTCMOS) [9]. It effectively reduces Pst by disconnecting the power supply through the use of high *Vt* MOSFET switches. However, there are serious drawbacks with the use of this technique, such as the fact that both memories and flip-flops based on this technique cannot retain data. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) [10] that reduces Pst by increasing the substrate-biases. This technique also faces some serious problems, such as a large area penalty and a large power penalty due to the substrate-bias supply circuits requires low leakage power.

IV. IMPROVED SELF-CONTROLLABLE VOLTAGE LEVEL CIRCUITS:

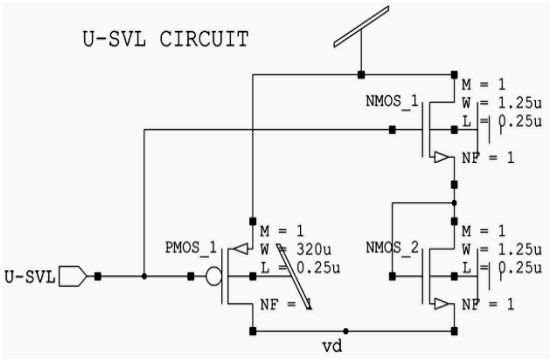

Figure 4. Upper SVL circuit

In the above figure shows Upper svl circuit. The impedance of a mos transistor increases with the width of the transistor.pmos1 in the above circuit having width means it offers very high resistance in that path between vdd and vd. So that leakage in this svl mode is very less. And also nmos1 and nmos2 forms a working in normal mode of the cell.nmos2 acts as a resister to reduce current in active mode. by connecting above way the leakage is further reduced.

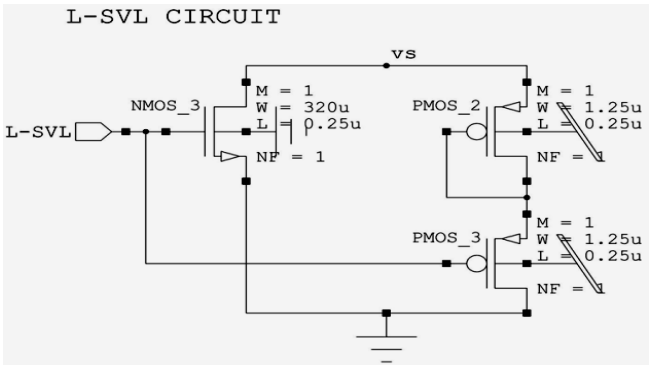

Figure 5. Lower SVL circuit

In the above circuit represents lower svl circuit.nmos3 work in the svl mode and pmos2 and pmos3 work in the normal mode of the cell.pmos2 acts as a resister to reduce leakage. These two techniques reduce leakage current compared to the previous svls.

TABLE II. 9T SRAM CELL SVL OPERATION

Mode	Upper SVL Circuit	Lower SVL Circuit
Active	pMOS switch is turned on	nMOS switch is turned on
	VDD is supplied	Vss is supplied
Stand-by Mode	nMOS switch is turned on	pMOS switch is turned on
	V_D ($<V_{DD}$) is supplied	V_S($>V_{SS}$) is supplied

V. 9T SRAM CELL WITH NORMAL SVL CIRCUITS:

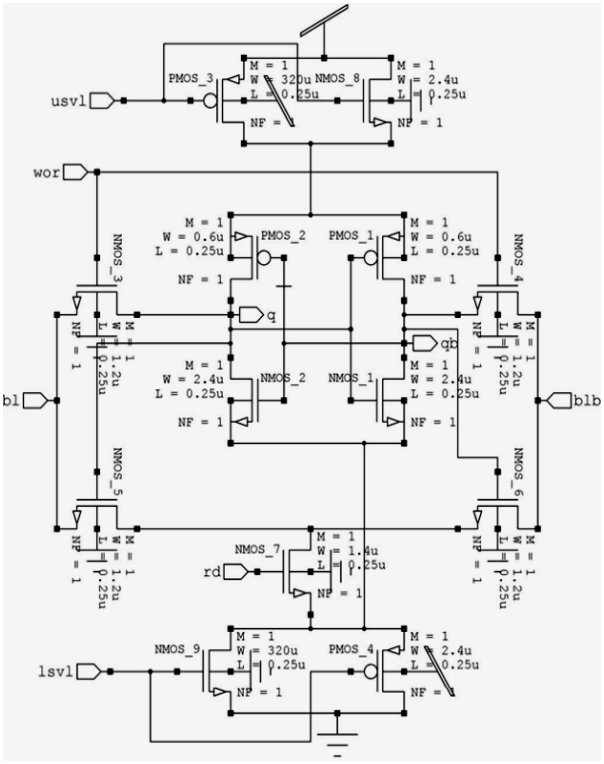

Figure 6. 9T SRAM cell with normal SVL circuits.

The above circuit work with normal svl circuits. The circuit consists of normal 9t sram cell and upper svl circuit and lower svl circuits and operation of the circuit explained With the table below.

TABLE III. 9T SRAM CELL OPERATION WITH SVL

u-svl	l-svl	wr	rd	bl	blb	qbar	q	operation
1	0	0	0	x	x	0/1	1/0	hold
0	1	0	1	1	1	0/1	1/0	read
0	0	1	0	0	1	1	0	Write0
0	0	1	0	1	0	0	1	Write1

The role of svl circuits is to reduce leakage currents in standby mode or hold mode because so much leakage power in stand by mode can destroy the cell. So we need to reduce that leakage. The proposed improved svl circuits can reduce leakage more. By observing the table for inputs logic 1 and 0 to the svl circuits we can say that the cell operates in hold mode. In this mode nmos8 on in upper svl circuit and pmos4 on in lower svl circuits to reduce the leakage.

VI. PROPOSED 9T SRAM CELL WITH IMPROVED SVL CIRCUITS:

The circuit in fig-7 reduces the leakage power in standby mode to protect the cell. The operation of the cell explained with the help of table above.nmos9 and pmos3 and also to reduce leakage further pmos4 and nmos10 is placed. In other modes the cell operates as normal operations read, write. In write mode svl provides expansion of the noise margin.

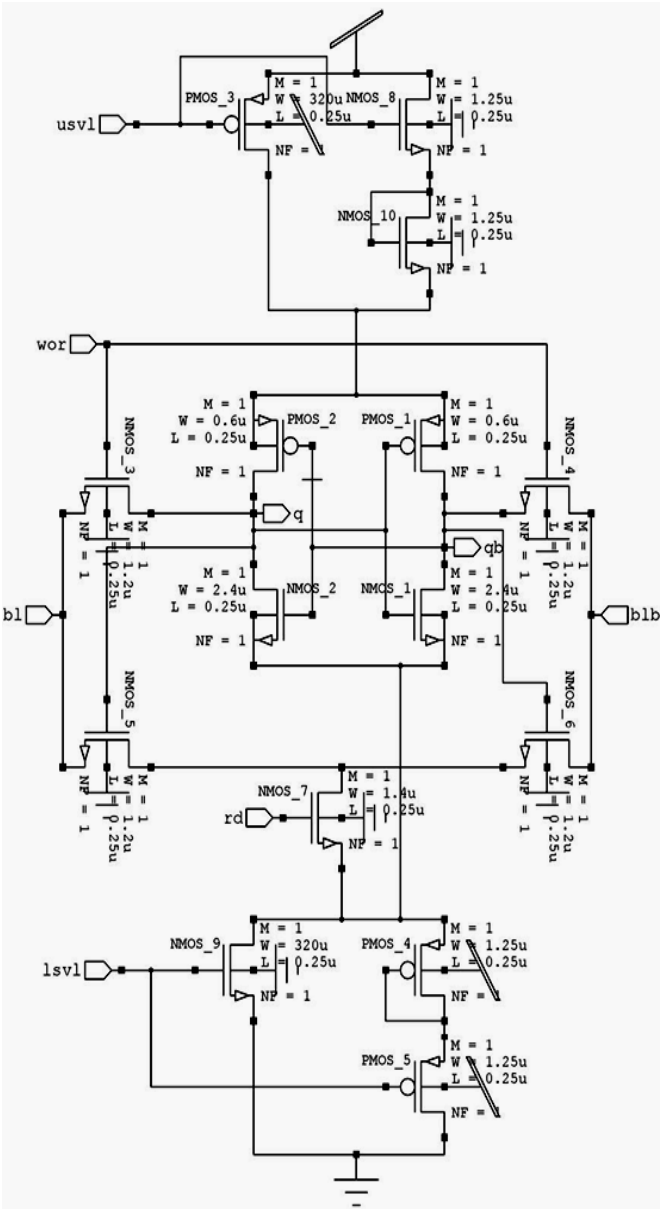

Figure 7. 9tT SRAM cell with Improved SVL circuits

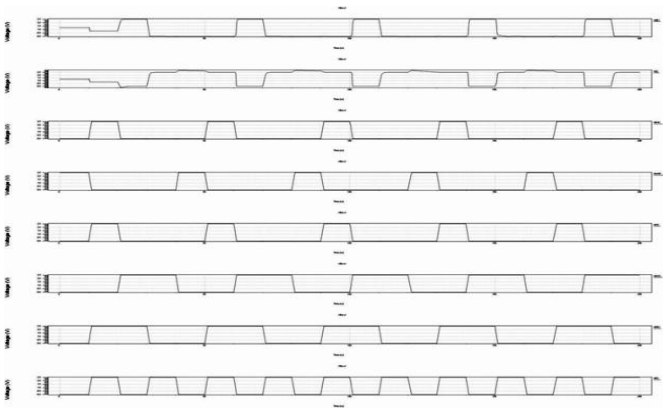

Figure 8. Simulation of 9T SRAM cell with Improved SVL circuits

VII. LAYOUT

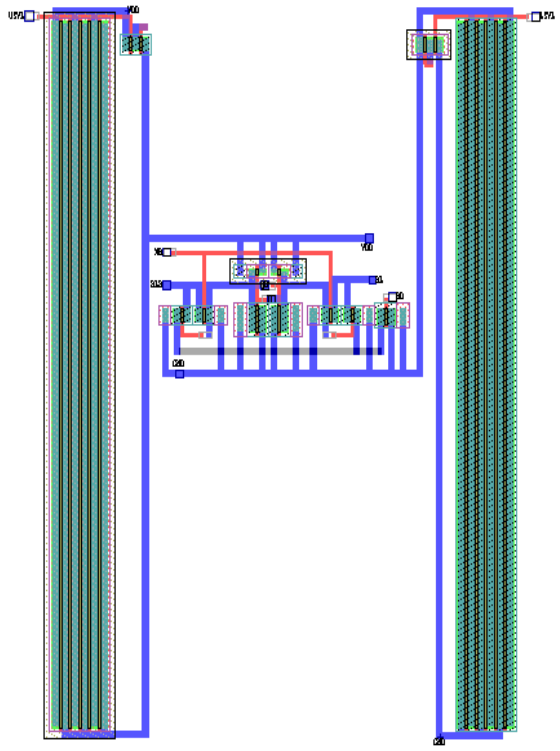

Figure 9. layout of 9T SRAM cell with Improved SVL circuits

The layout of the above figure shows 9t with svl protection circuit. Most of the area occupied by using w=320um svl transistors. The above layout uses two metals and 320um transistors can with connecting five transistors in series with a width of 64um.and the other transistors are connected according to the design values.

VIII. SIMULATION RESULTS

A. *Static Noise Margin*

Adobe Photoshop CS8 tool was used for rotation purpose. We have done this project by Tanner 13.0 version tool. Practically we can't get butterfly structure that is why we rotated the graph according to x-y coordinates. Finally we got butterfly structure as shown in figure below. Since by knowing the diagonals of the maximum embedded squares we can calculate the sides. The squares have maximum size when the lengths of their diagonal D1 and D2 are maximum the extremes of this curve correspond to the diagonals of the maximum embedded squares [4].

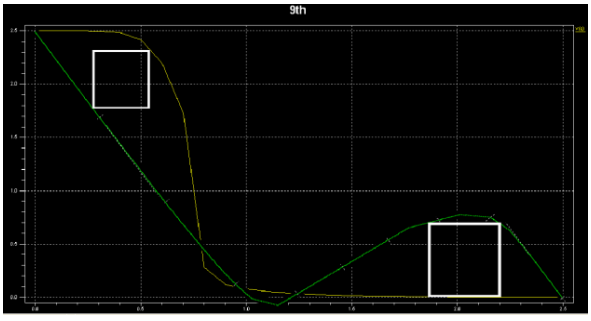

Figure 10. 9T SRAM cell static noise margin

TABLE IV. STATIC NOISE MARGIN COMPARISION

SNM	9TSRAM	9T Improved svl circuits
Hold	0.6 v	0.6 v
Read	0.6 v	o.7 v
Write	0.65 v	0.8 v

B. *Leakage power:*

1) *9T SRAM cell:*

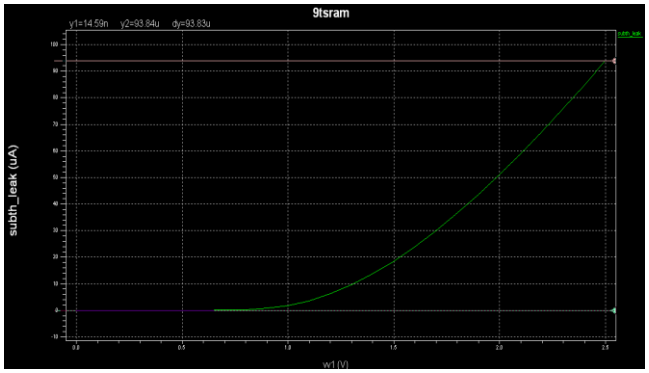

Figure 11. 9t sram cell leakage current

2) *9T SRAM with normal SVL circuits*

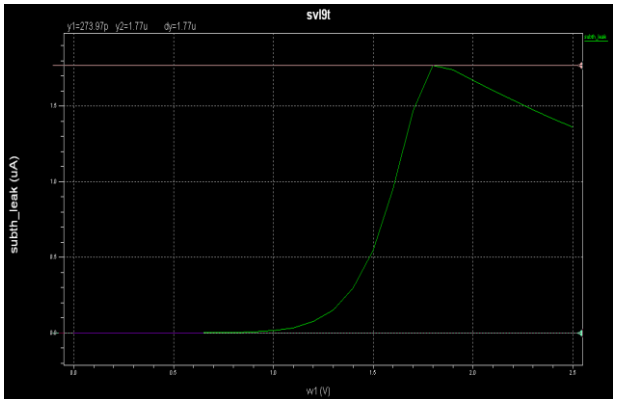

Figure 12. 9T SRAM cell with normal SVL leakage current*3)9T SRAM with Improved SVL circuits*:

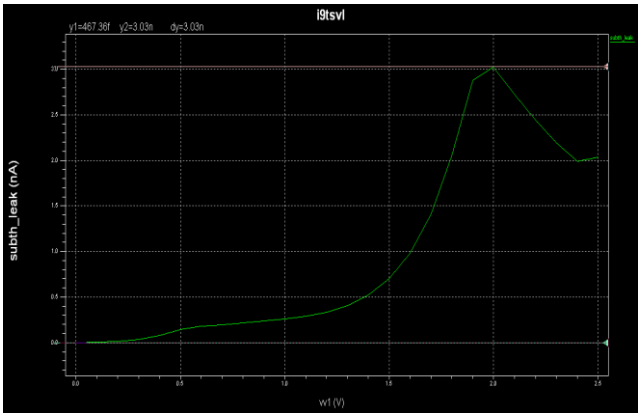

Figure 13. 9T SRAM cell with improved SVL leakage current

TABLE V. LEAKAGE POWER COMPARISION

VDD=2.5V,CL=1fF	Leakage power
9Tsram cell	234.574 uw
9T normal svl cell	4.425 uw
9T improved svl cell	7.575 nw

C. Power dissipation:

TABLE VI. POWER DISSIPATION COMPARISION

	Power dissipation
9Tsram	1.363e-004 w
9T normal svl circuits	7.493e-005 w
9T with improved svl circuits	4.49e-005 w

TABLE VII. PROPAGATION DELAY COMPARISION

D. Delay

Propagation delay	9T Sram	9T improved svl circuits
Hold	2.0491e-011	2.4752e-011
Read	2.1625e-011	2.0048e-011
Write	2.2405e-011	2.2448e-011

E. Area

	Area(μm²)
9Tsram cell	118.798
9T improved svl cell	1126.57

IX. CONCLUSION AND FUTUREWORK

Improved SVL circuit will play a major role in future. The effect of the improved SVL circuit on the leakage current through the load circuit (i.e., reduction in current) was examined. The improved SVL circuit and the load circuit were designed using 0.25μm CMOS technology. Sub-threshold memory design has received a lot of attention in the past years, but most of them use large number of transistor to achieve sub threshold region operation. The new technique inherently process variation tolerant, this makes the new approach attractive for nano computing in which process variations is a major design constraint. In this circuit we have several advantages in different modes that is in operating mode high V_{ds} to load circuits for high speed operation, in stand-by mode high V_t through "On MOS switches" to load circuits for minimum stand-by leakage power, data retention, high noise immunity, small stand-by power dissipation, negligible speed degradation, negligible area overhead, high noise immunity, data retentions at stand-by mode. In this circuit the standby leakage power is reduced by which total average power also reduced.

ACKNOWLEDGMENT

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